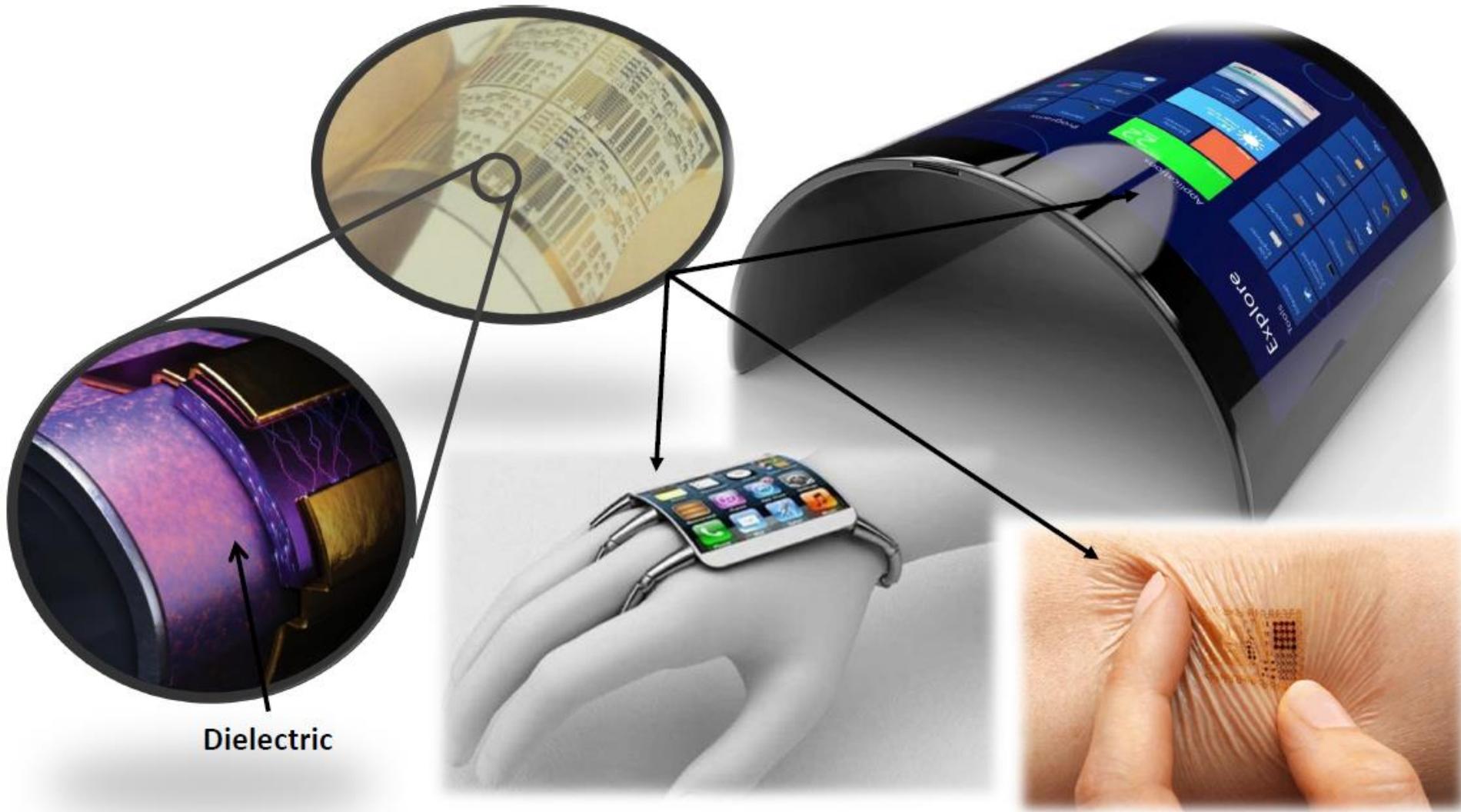


Highly Reliable Organic Non-Volatile Memory Devices Based-on Hybrid Films via iCVD Process

Dankook University
School of Electrical & Electronic Engineering
Prof. Min Ju, Kim

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1. Introduction
2. Hybrid Films via initiated Chemical Vapor Deposition Process
3. Resistive Switching Behavior of Hybrid-based 2-Terminal Devices
4. Charge Trapping Non-volatile Memory Devices with Band Engineered Hybrid Gate Stacks



- ✓ The dielectric is a key component that determines the performance of flexible electronics



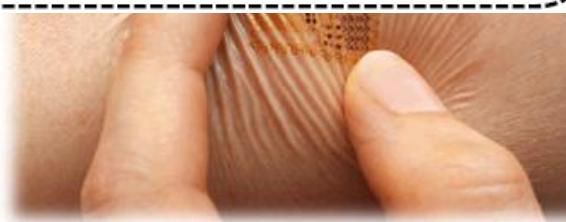
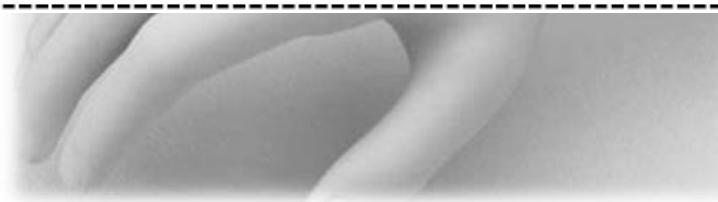
- Need to develop flexible high-k dielectric materials
- Demand for the use of a new process, called initiated chemical vapor deposition (iCVD)



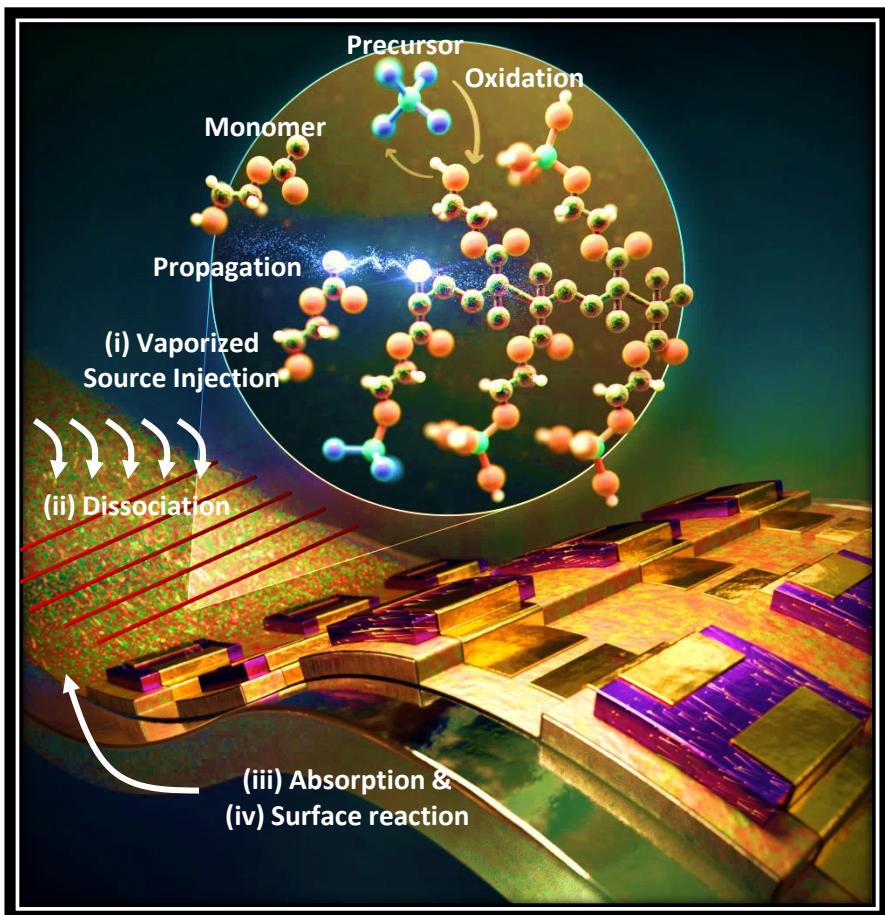
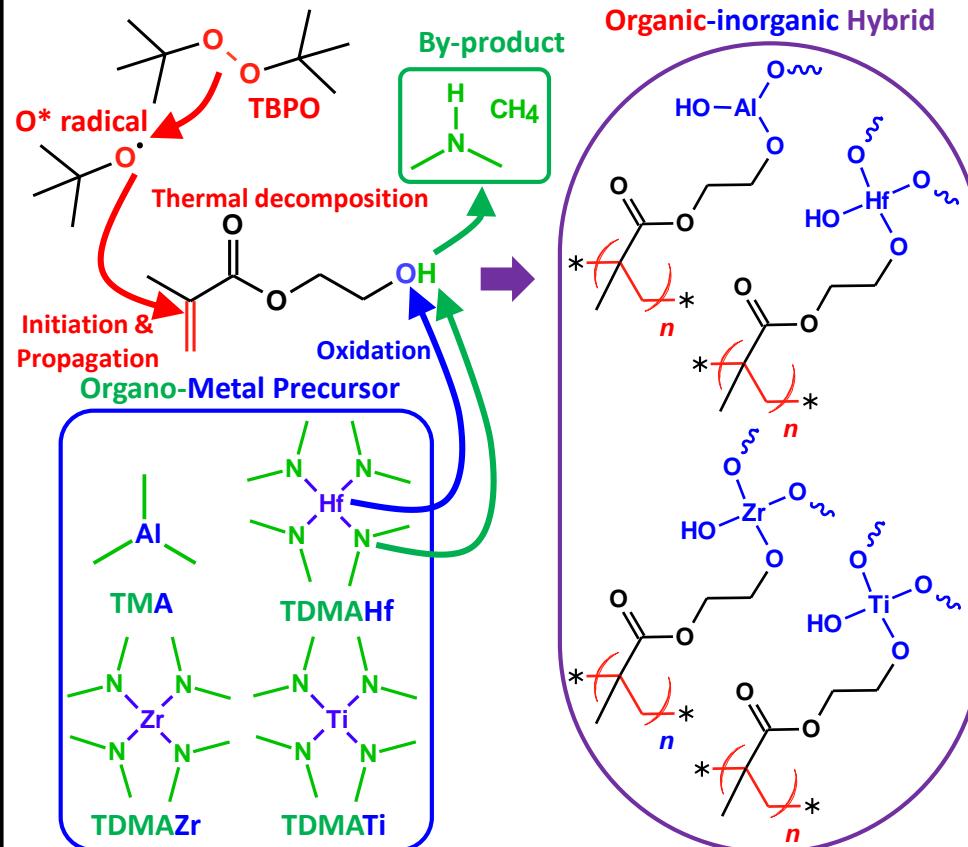
- Karen K. Gleason (MIT) who is Mother of iCVD process
- Prof. Im adapt iCVD process into Korea (2010)



Dielectric



- ✓ The dielectric is a key component that determines the performance of flexible electronics

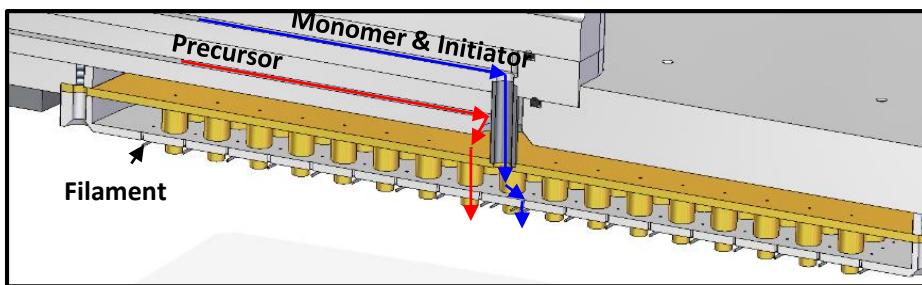
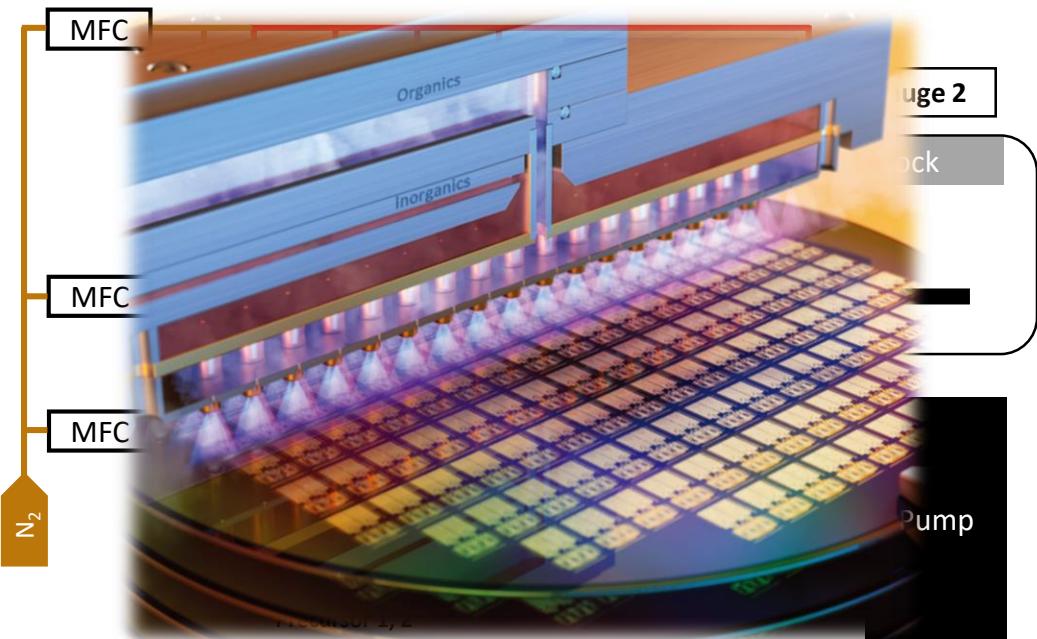
Process Scheme*Synthesis Mechanism*

- ✓ Synthesis of AlO_x , HfO_x , ZrO_x , and TiO_x contained hybrid dielectrics with systematical comparison
- ✓ The **oxidation reaction** between the hydroxyl (-OH) functionalities in the monomers and precursors
→ Formation of **metal-oxide moieties** in the polymer matrix

2. New Chamber

New Geometry of iCVD Chamber

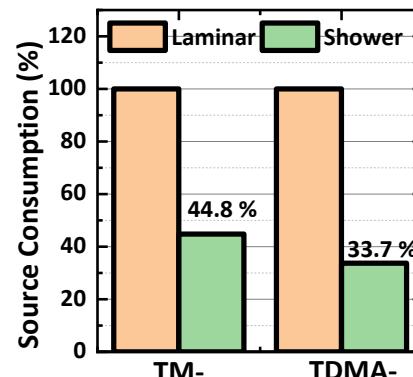
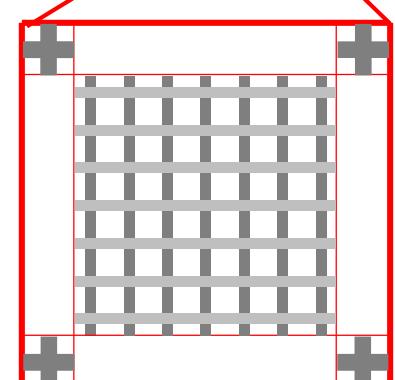
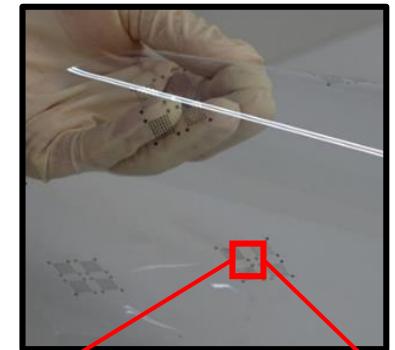
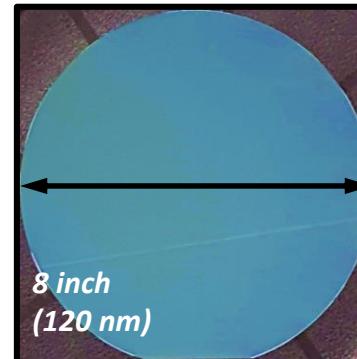
Geometry of New Chamber



✓ New geometry design of iCVD chamber for large-area, uniform, conformal, homogeneous deposition of hybrids

- Dual shower-head structure module
- Evenly divide and spread vaporized sources
- Prevent non-surface reaction between sources
- Covering entire 8-inches

Large-Area Scale Deposition

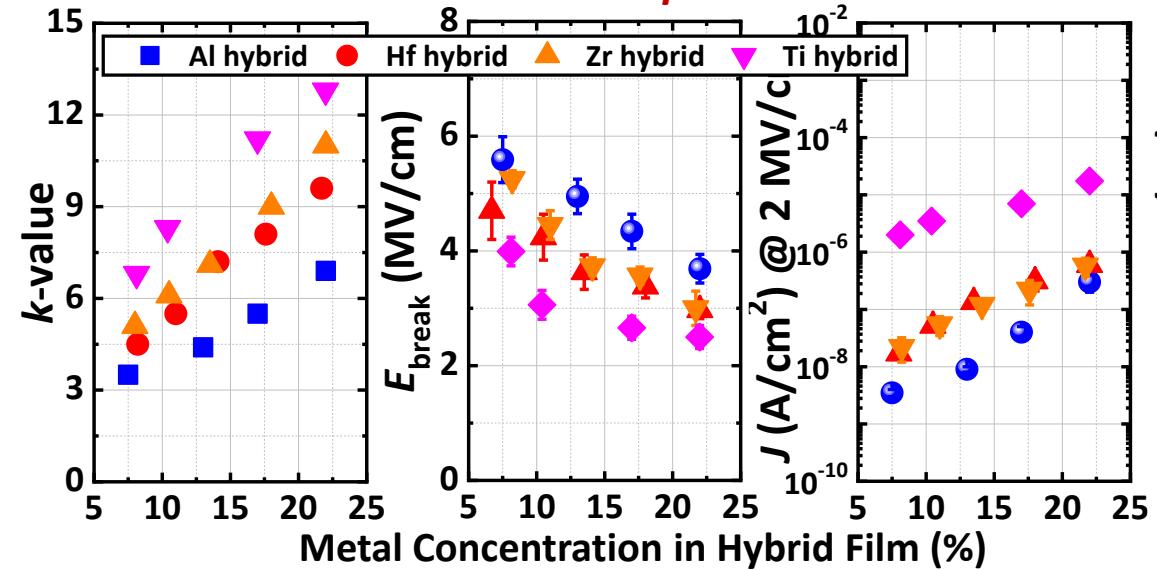


Macromolecular Materials & Engineering, 306 (3), 2000608, 2021, (Journal Cover)

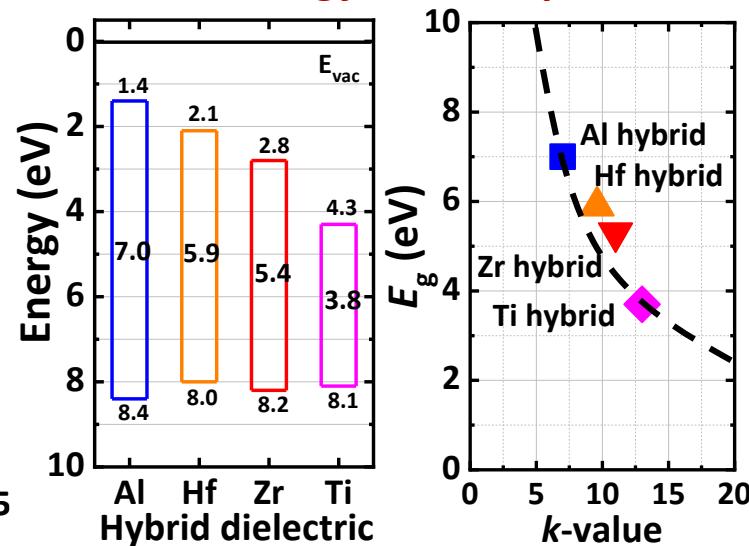
2. High-k Hybrids

Electrical Properties

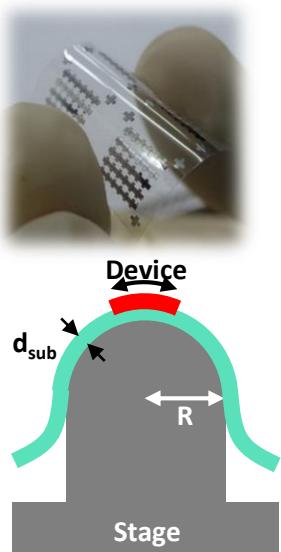
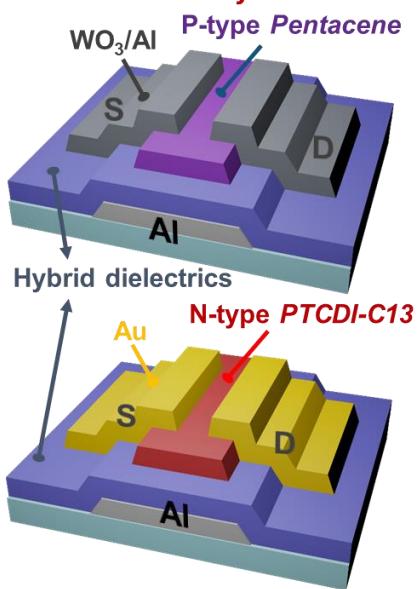
Dielectric Properties



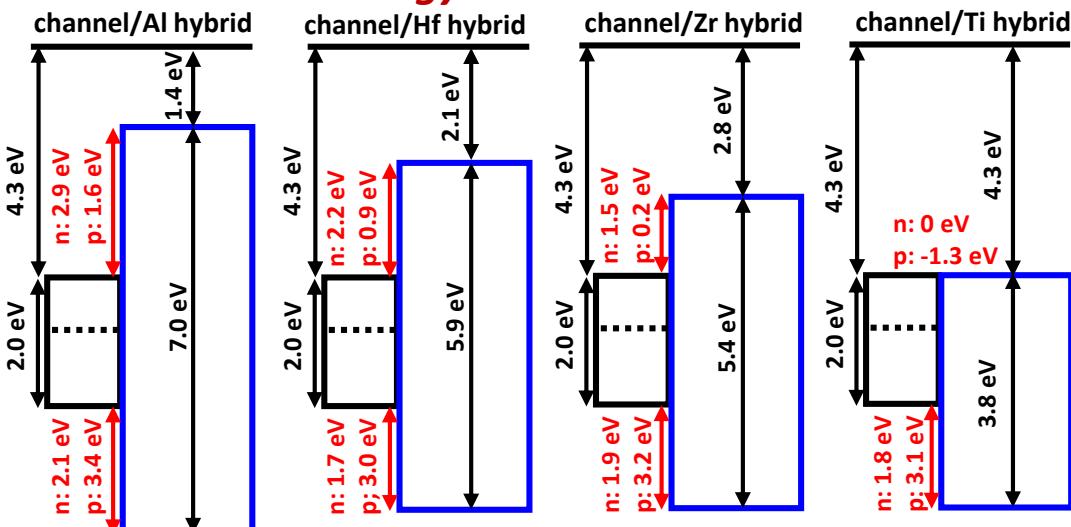
Energy Band Gap



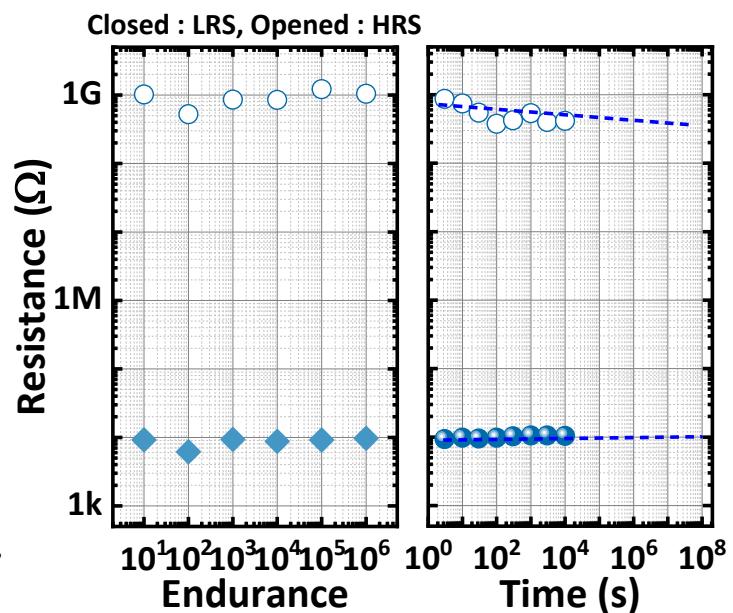
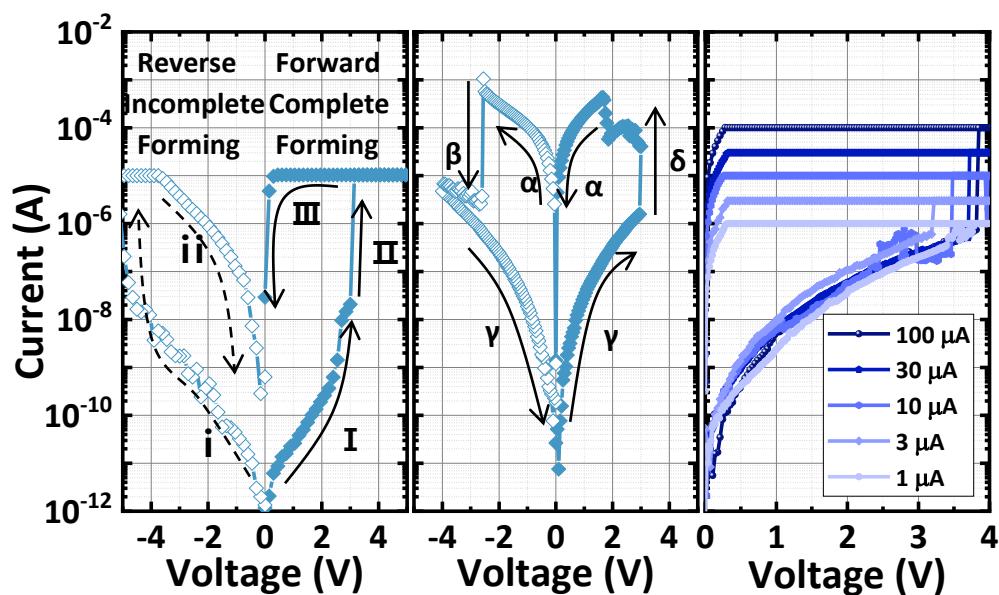
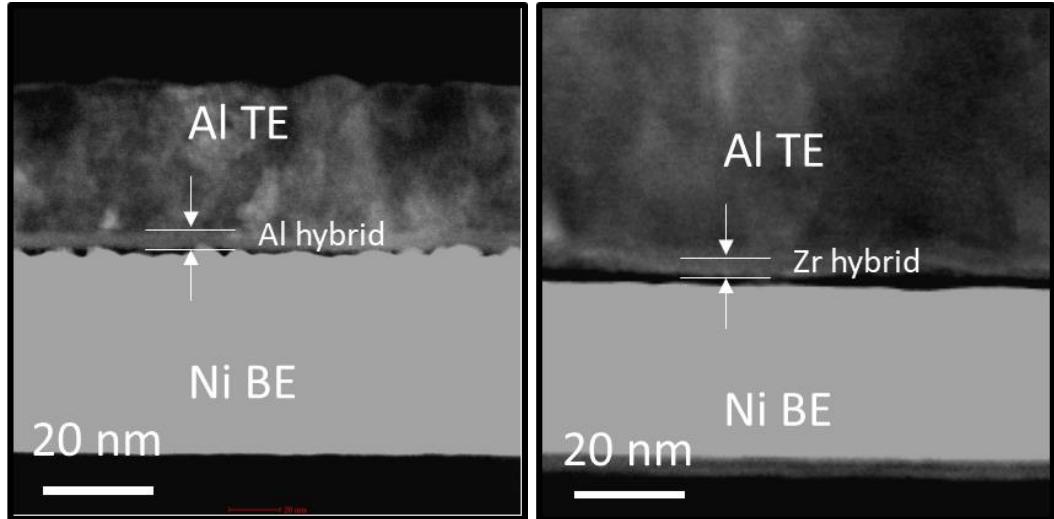
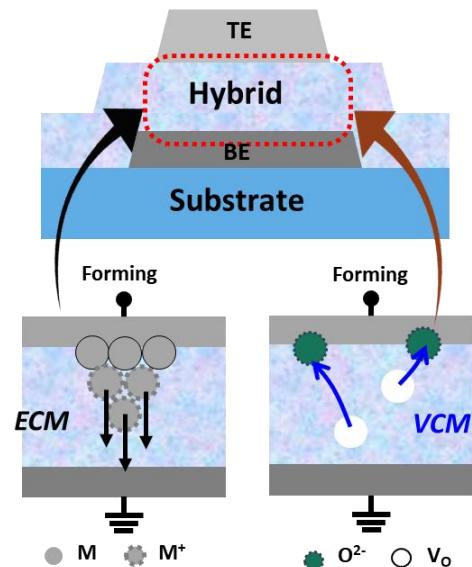
Structure of OTFTs



Energy Band Structure

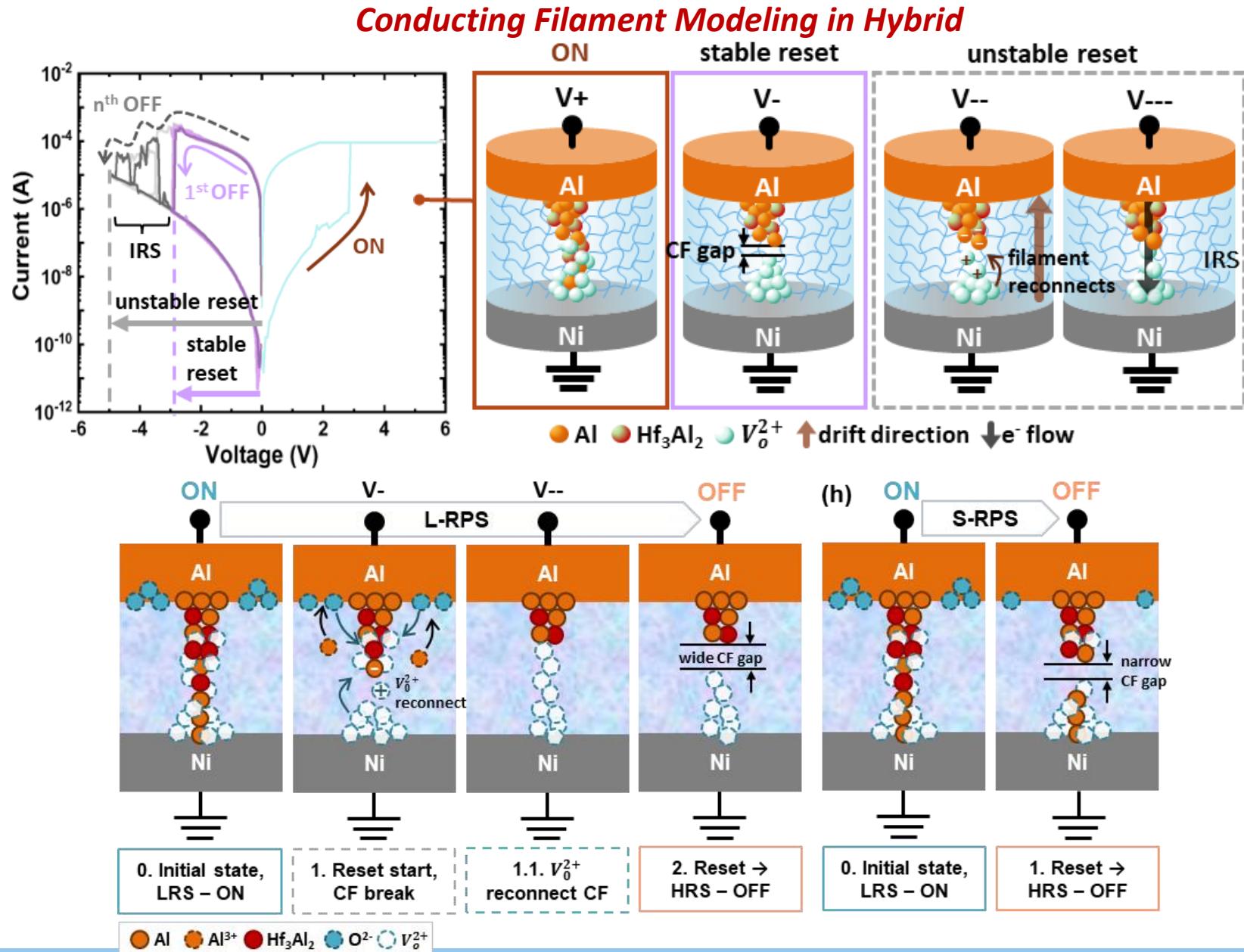


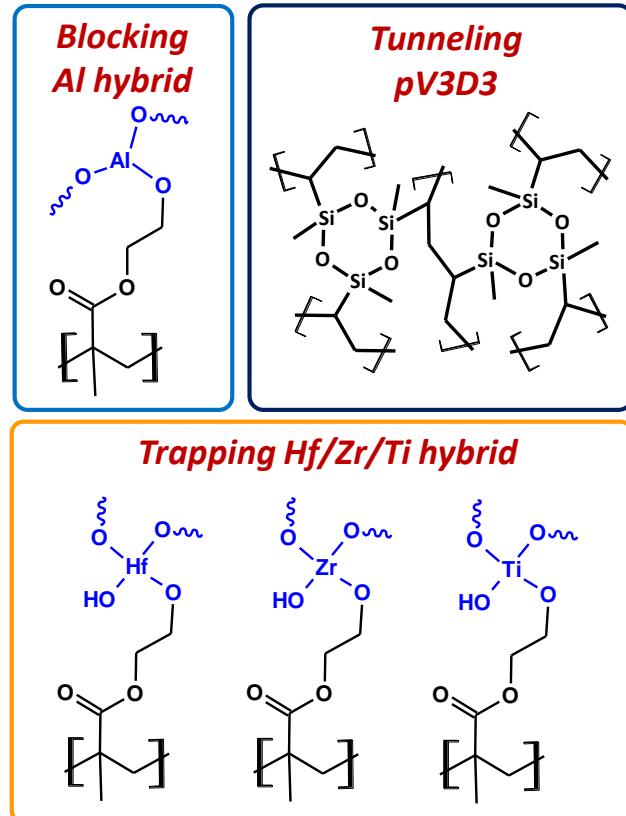
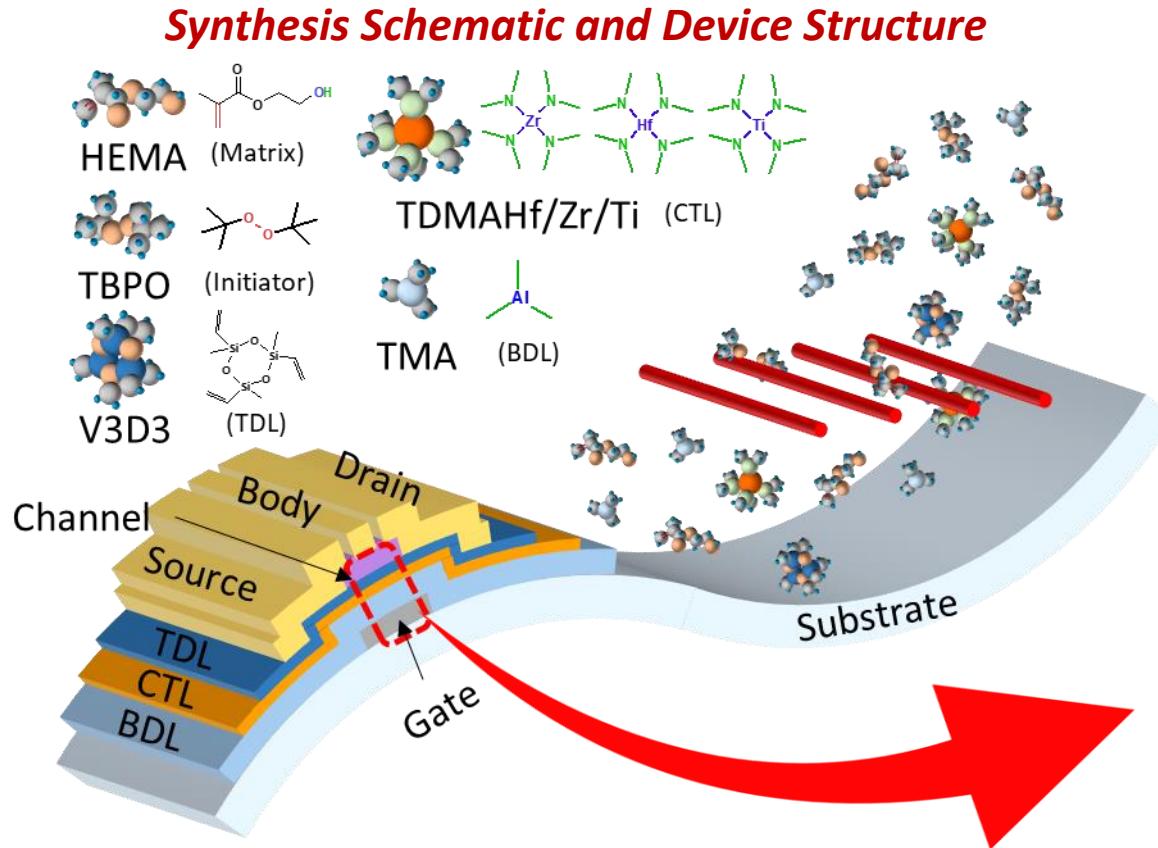
Resistive Switching Behavior of Hybrid-based ReRAM



3. Resistive Memory

Conducting Filament Modeling of H-ReRAM





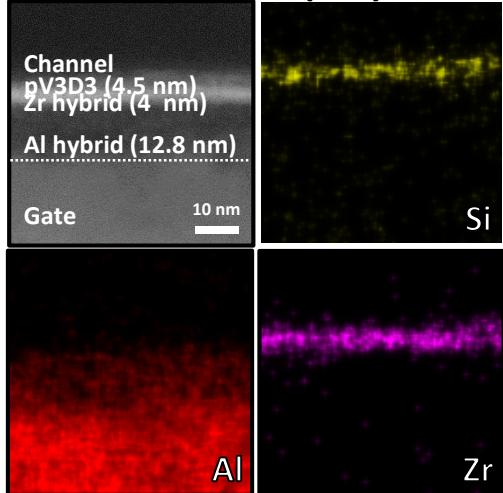
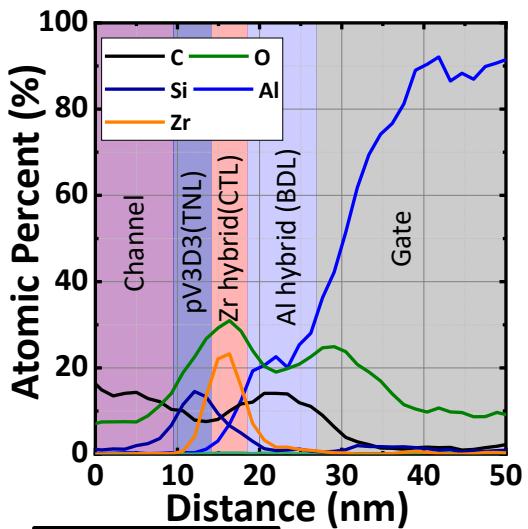
- ✓ Bottom-gated OTFT-based CT-ONVM device
 - Blocking dielectric layer (BDL) : Al hybrid (Wide E_g , **high- $k=5.0$**)
 - Charge trapping layer 1 (CTL1) : Hf hybrid (Narrow E_g , **high- $k=7.5$**)
 - Charge trapping layer 2 (CTL2) : Zr hybrid (Narrow E_g , **high- $k=9.0$**)
 - Charge trapping layer 3 (CTL3) : Ti hybrid (Narrow E_g , **high- $k=6.0$**)
 - Tunnelling dielectric layer (TDL) : pV3D3 (Wide E_g , **low- $k=2.2$**)
 - Channel : C13-PTCDI (n-type), pentacene (p-type)

- **High Band offset**
- **E-Field maximization in TDL**
- **Charge trapping efficiency enhancement**

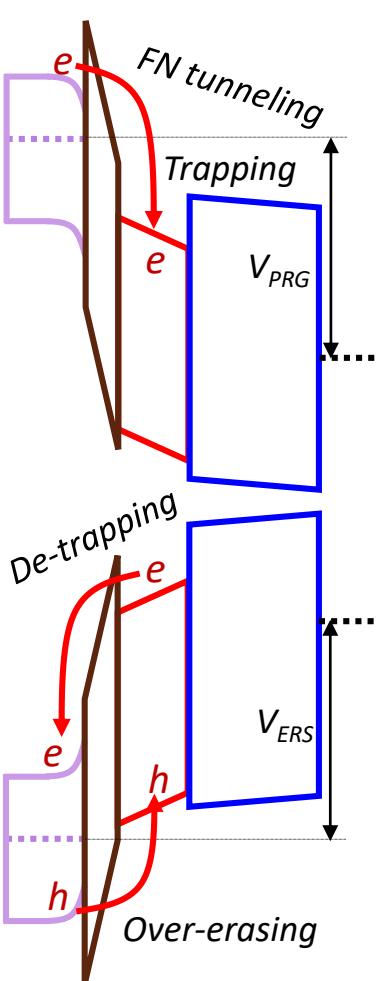
4. Charge Trapping Memory

Program(PRG)/Erase(ERS) Behavior of CT-Hybrid-ONVM

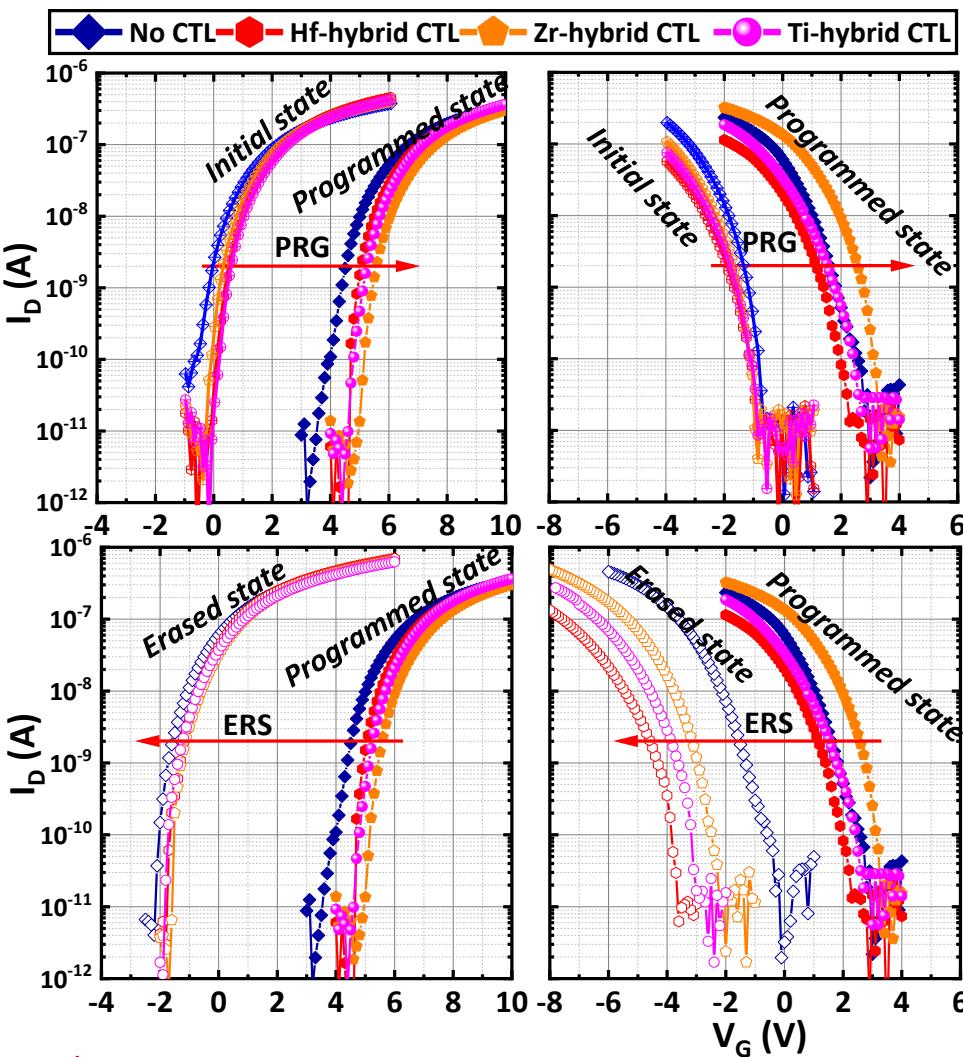
TEM + EDS Images



Energy Band Bending



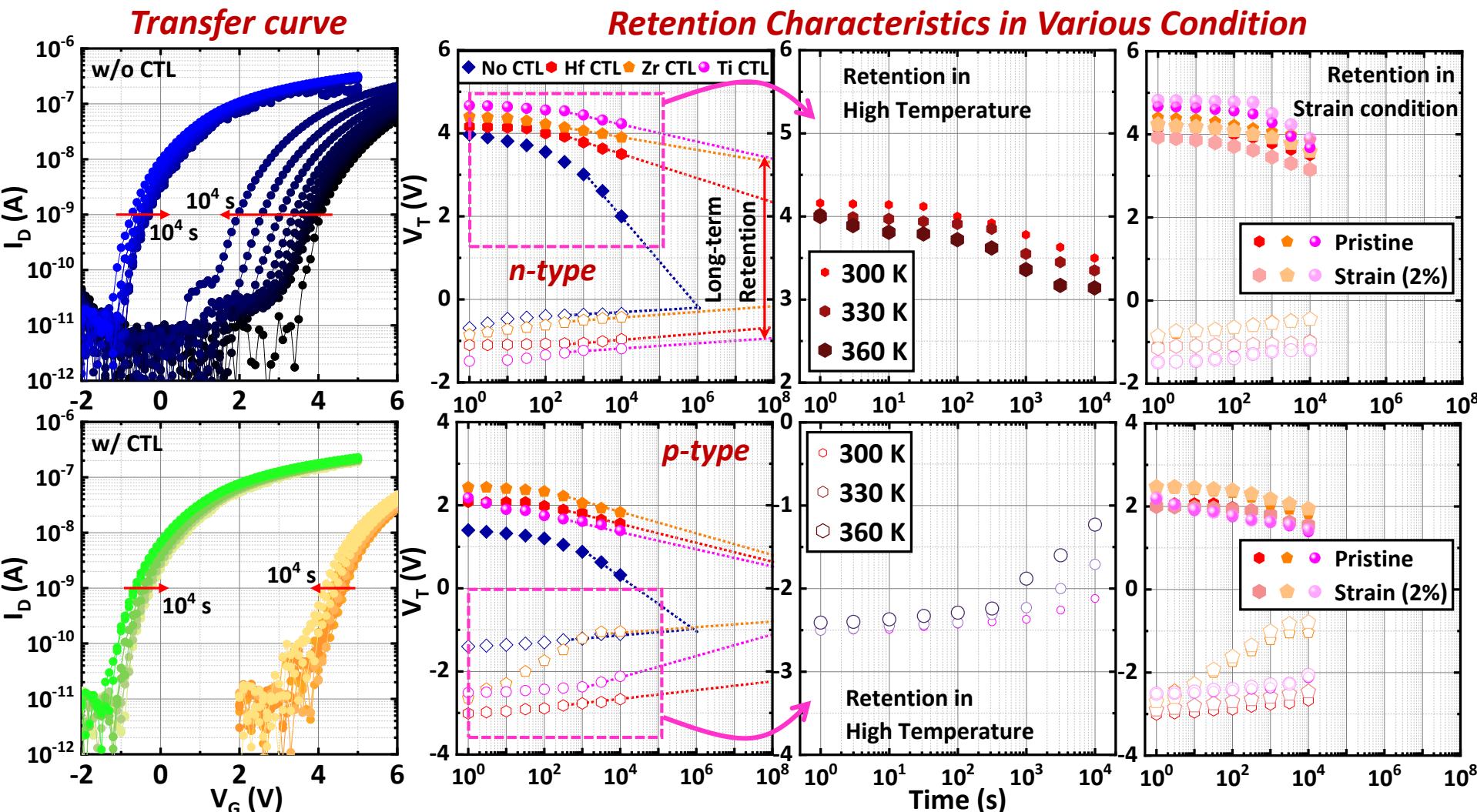
Transfer Characteristic in PRG/ERS



- ✓ Ideal transfer characteristics with **hysteresis free** and **low-voltage operation**
→ Advantageous in **non-distorted Read** operation
- ✓ Incremental step pulse programming/erasing (ISPP/ISPE), PRG/ERS speed, Endurance, and Retention

4. Charge Trapping Memory

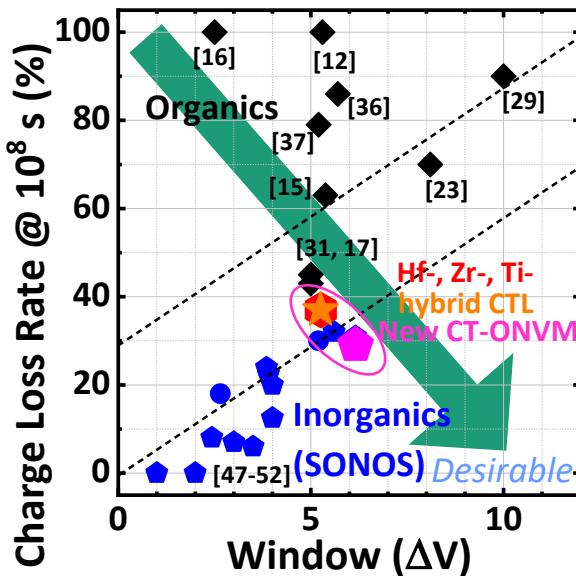
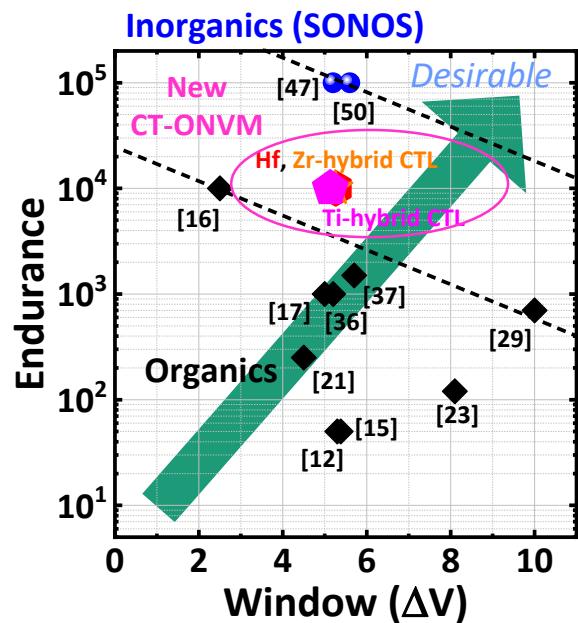
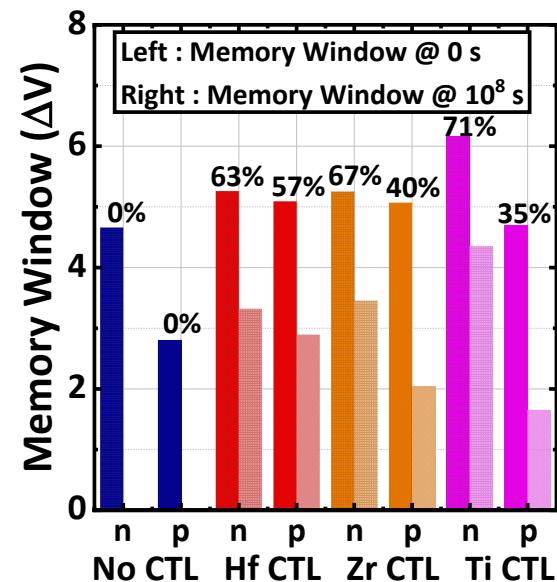
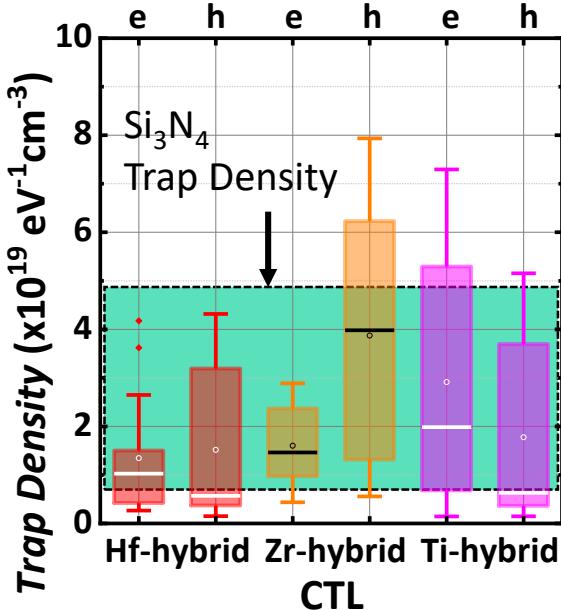
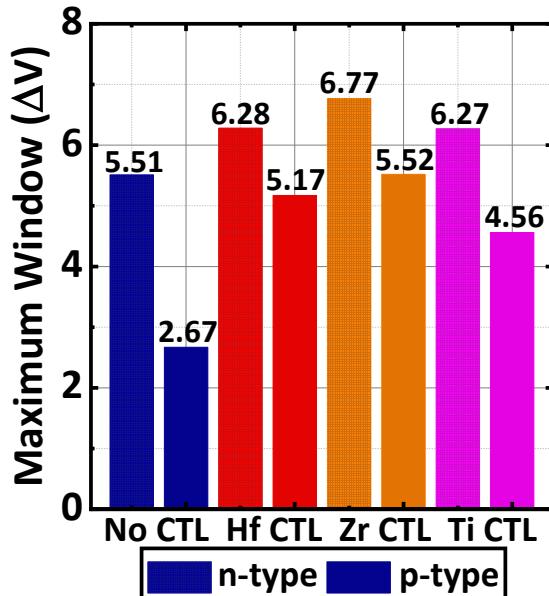
Retention Characteristics



- ✓ W/o CTL → Dramatic charge loss along with time, W/ CTL → Prevent charge loss to maintain V_T
- ✓ Retention properties in high temperature condition (for calculating trapping density in CTL; next page)
→ Deep electron potential well, Shallow hole potential well
- ✓ No difference in retention between the pristine and the strained condition

4. Charge Trapping Memory

Benchmarks



Thank You for Attention !